**Reminiscing my days at the Vikram Sarabhai Space Centre (VSSC), Trivandrum.**

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1. **My Early Life and Education**

I was born and raised in a middle class family in Calcutta and had my schooling at the St. Xavier’s Collegiate School. I passed my School Final Examination from the West Bengal State Board with a rank and a scholarship in 1959 which entitled me to free education during my two years of I.Sc. studies at the Presidency College, Calcutta. I went on to complete my B.Sc with Honours in Physics from the same college and in 1963 joined the Institute of Radiophysics and Electronics at the Calcutta University Science College Campus to complete my B.Tech and M.Tech. degrees. Thereafter I joined a research group at the same institute working on Switching Theory. This was my first introduction to the study of digital computers which in those days was looked upon with both awe and fear. It may be noted that I did not have any formal course on the subject during my studies and whatever little I have achieved in life has been due to a learning process in my work place inspired by some great personalities who came into my life at the VSSC in Trivandum. Our university education in those days taught us how to learn on our own rather than impart some knowledge by rote.

1. **Journey to Kerala**

When I moved to Trivandrum in 1968 from Calcutta as an engineer at the Thumba Equatorial Rocket Launching Station (TERLS), I must admit that I felt immensely home sick. Born and raised in an urban milieu with a strong Bengali flavor, I found it very difficult to come to terms with the way of life in Trivandrum of those days. An intensely rural town had little space for a first generation Calcuttan. Little did I know that TERLS would morph into the gigantic and wonderful Vikram Sarabhai Space Centre (VSSC) in its formative years. Trivandrum became my home for the next 34 years till 2002, my year of superannuation. VSSC became my work place where I found the best mentors, the most precious friends and a set of devoted and committed colleagues all of whom combined to present tome the greatest gift of life i.e. a beautiful existence. But all of this would not have been possible without a creeping feeling of commonality with the ethos of Kerala during my first two years of loneliness. I could realize that there after all was a strong bond between my home state of West Bengal and my adopted state of Kerala. My analysis revealed that both the peoples loved three very disjoint things in life. Our food habits made fish a must in our eating patterns. The romanticism associated with a class of political belief was another strong common factor. And in sports the love for football which I found among the Keralites of the late sixties gave me reason to believe that if there could be a second home for me then it must be Kerala. Be that as it may, some of the luminaries of rocket science who till today have been my greatest source of influence have been. Dr. Vikram Sarabhai, Prof. Satish Dhawan, Dr. APJ Abdul Kalam, Dr. SC Gupta, Dr. UR Rao, Dr. K Kasturirangan, Dr. S Sreenivasan and Dr. G Madhavan Nair. I cannot complete this essay if I have to write about how each one of them inspired me in my workplace. Suffice to say that generally speaking it was their way of life more than anything else that must have encouraged me to learn new technologies and methods and thereby build the systems that I did. However I must mention about Dr. Sarabhai after whose name the centre was christened after his untimely death on the 30th. December, 1971. I had seen him from a distance during his frequent visits to TERLS during the period. Clad in Kurtha and Pyjamas and with an ever smiling face, he would move about the place alone going from office to office and enquiring about the staff as if they were known to him for a long time. He would chair review meetings and try to understand what we proposed to do and how the projects fitted into his vision of making India the space power it is today. I still remember that he would drink tender coconut water during the meetings and not the usual beverages of tea and coffee. His last visit to Trivandrum was in connection with the inauguration of the Thumba railway station. On the morning of the fateful day when we went to office we were told that Dr. Vikram Sarabhai was no more and that he had passed away in his sleep the previous night after attending meetings with senior members of our staff till late at night. He died only to gain immortality through the existence of the Vikram Sarabhai Space Center, one of the greatest and successful research institutes in the country which till today has been the bedrock of development of intricate rocket systems that have given credence to the belief that India is mature in the design and development of launch vehicles.

1. **My first assignment at TERLS**

My first assignment in 1968 at TERLS was to design logic circuits and thereby acquire a capability to build the On Board Processor (OBP) systems that would be used in the navigation, guidance and control systems of the launch vehicles that the centre would have to build in the days to come. My boss was Dr. SC Gupta who was the Head of the Control and Guidance Division in those days. Dr. Gupta has been my chief mentor during all my years at VSSC. His analytical mind, unassuming behavior and above all the air of being a perfect gentleman have all left a lasting impression in my mind.

It was an era when integrated circuits (ICs) in their most primitive forms (like a Quad 2-input NAND gate or a Dual J-K Flip Flop) were making waves and I can still recollect the excitement that overwhelmed us when the first consignment of ICs arrived in our laboratory. That excitement is understandable because I had by that time gone through the mill of building a transistorized version of a full adder which occupied a printed circuit board space of about 10 square inches! Digital voltmeters were just coming into the market and were replacing the more ubiquitous vacuum tube voltmeters known as VTVMs. The present day acronyms such as RAM, PROM, ASIC, SCSI, PCMCIA, etc. made little or no sense to the most knowledgeable and the letter C had no more importance than its other 25 peers that constitute the building blocks of the English language. PNP was a jargon used to classify a transistor by the polarity of its majority carrier. The yuppies of today's electronics industry feel that PnP is an acronym best used to describe "plug and play". Mercifully, for sentimentalists of my generation, the letter "*n*" used by them is in italics. Or, if I am permitted to borrow a phrase from my younger colleagues, the acronyms have been chosen to be made case-sensitive.

Most of my colleagues including myself were products of an indigenous education system with no formal training in an overseas university. But we had our ears and eyes firmly rooted to our environment soaking in the knowledge that was needed to do our jobs meticulously. We did not shut ourselves from the world at large as we had arguably one of the best technical libraries in the country- again a result of the vision of Dr. Sarabhai. There was neither any internet nor was Google known at that time. But we used to get the hard copies of the IEEE Transactions and Proceedings of the IEEE regularly to keep us connected to the developed world. It was with this sort of a background we embarked on the design and development of the OBP systems which I am going to describe now.

1. **The Story of OBP Development at VSSC.**

The story of the development of On Board Processors (OBP) at VSSC has always been related with the decision to deploy a closed loop inertial navigation and guidance system for a particular launch vehicle.. As must have been explained elsewhere such a system requires that the velocity and position of the vehicle are computed on board in an OBP by sensing the linear and angular movements of the rocket and determining in real time any correction that may be required to the sensed trajectory in case of any deviation. The corrections were sought to be issued in the form of commands to the vehicle autopilot system. Thus with these broad goals in mind the development of the OBP system began in the early 1970s. Realizing that the development of such a system may evolve with the development of computer technology at the global level, the first such attempt was christened OBP MKI.

OBP MKI

This was built using medium power DTL and TTL technology for the central processing unit (CPU) and the processor bus and magnetic core for the memory having a 5 microsecond cycle time. The word length of the machine was 20 bits and it had about 30 odd instructions. It may seem odd that a word length of 20 bits was ever thought of. But it must be remembered that in the early ’70s the concept of byte being a unit of data was not as well established as it is today. However this choice of 20 bits for the word length was made after a lot of deliberations with the designers of the navigation and guidance systems who felt that a precision of 20 bits would suffice for the SLV3 launch vehicle. It has to be remembered that building a floating point hardware was not even contemplated and the legacy of using fixed point arithmetic continued even in the ongoing missions. Described in this article. The CPU was built around a microprogrammed control unit and the entire microprogram was hand coded by VSSC engineers.

The machine was built as a laboratory model in 1974 and it functioned well in the comfortable environment of the laboratory. Further development of OBP MKI was abandoned soon thereafter with the decision to have an open loop guidance system and analog autopilot for the SLV3.

While this was a minor setback for the engineers who developed the system, it nevertheless gave them a lot of insight into the building of complex hardware. It is instructive to point out that the software for the machine was written entirely in machine language as tools such as compilers, assemblers and linkers were yet to be developed.

However with the decision to adopt an open loop guidance system, the engineers involved in the design of OBP MKI had to rise to the occasion and develop an embedded system known as the Vehicle Attitude Programmer (VAP).

VAP

This was built as a 2 unit system known as

1. a rate multiplier unit and
2. a rate storage unit.

The rate multiplier unit was used to digitally integrate its inputs obtained from the rate storage unit and to output the result to the vehicle autopilot system. The rate storage unit which was a plug in unit to the rate multiplier unit consisted of a bipolar programmable read only memory (PROM) of capacity 64\*8 in which was stored the pitch rate segments for the particular mission.. Essentially what this means is that the output of the VAP was a predefined pitching profile of the launch vehicle. Thus by just altering the contents of the PROM, a new open loop mission for the SLV3 could be defined. While all this may seem to be trivial from the perspective of today’s hardware technology, it has to be remembered that the design, development and deployment of the VAP took place during 1974-1983 when the technology of microprocessors even in its most primitive 8 bit form was not known.

OBP MKII

1. The Background

With the successful culmination of the SLV3 series of flights in 1983, the sights were set on a more advanced ASLV launch vehicle with a clear mandate that adoption of a closed loop inertial navigation and guidance system and use of digital autopilot would be one of its most important goals. Thus the designers of OBP MKI were asked to develop a reliable OBP system which would form the basic hardware platform on which such a system would be built. It was back to the design review committee to select one among the many options that were there. However, with the availability of 8 bit microprocessors and associated development tools such as in circuit emulators and logic analyzers, the committee did not feel it was necessary to repeat the strategy of OBP MKI. Time was short and the system had to be developed fast. However since this OBP system would be a mission critical one, it was mandated that the OBP MKII would have redundancy in the form of a hot standby computer so that all single faults in the system would not lead to mission failure. In other words the system was designed to be a single fault tolerant one. It was also necessary to augment the power of the microprocessor to cater to the demands of high speed integer multiplication and division. While selecting the technology, it was decided that reliability would be the single most important factor which would dictate such a choice. Thus components to be used for such a mission critical hardware must conform to stringent military standards, must have had a good record of use in similar applications elsewhere and must pass through the rigorous screening tests that they would be subjected to in the components screening laboratory at VSSC. One of the consequences of this consideration was the choice of the microprocessor and memory devices. Motorola’s 6800 microprocessor may seem to be outdated today but at the time of finalizing the OBP MKII configuration for ASLV in the early ’80s, this was the only device that could satisfy all the criteria. Similarly the 2114 a 1K\*4 static RAM was chosen as the memory device because of its relatively long and successful record of use.

1. The Architecture.

Having decided on the redundancy mechanism and the choice of major components, it was necessary to examine the other architectural attributes for the given application. Since the dominant natural frequencies of the stabilization and control system of a launch vehicle are considerably higher than those of a navigation and guidance system, a higher computing speed was required for the autopilot algorithms. Typically two to four computing cycles per second were considered adequate for the ascent navigation and guidance of the launch vehicle, while fifty computing cycles per second were sufficient for the flight control. With the above considerations in mind, the main computing cycles for the OBP were split into two and were known as

* + Major Cycle.----every 500 miliseconds. The algorithms of navigation and guidance were carried out once every major cycle.
  + Minor Cycle-----every 20 miliseconds. The functions of vehicle control, digital filtering and self check were implemented every minor cycle.

The architecture which supports this type of cyclic, iterative computations was based on a distributed and multiprocessing system. It had the following major features.

* A few basic building blocks or modules.
* Parallel bus for intraprocessor data flow.
* Serial bus for inter processor data flow.
* A set of standard software modules.

An estimate was made of the computational load both in terms of execution time and memory capacity. From these estimates it was realized that the major number crunching operations should be carried out in a central processing system known as the Navigation, Guidance and Control Processor (NGCP). To protect the NGCP from electrical noise it was isolated from its environment by using optical isolators at its inputs and outputs. Therefore the basic tasks of input i.e. the data acquisition from sensors and output i.e. the data distribution to the actuators were sought to be carried out by separate Stage Processor Modules (SPM) located close to the sensors and actuators of the rocket. The transmission of data between NGCP and SPM would be via optically isolated serial links. It is worthwhile noting that the SPM which was located close to the navigation sensors was christened the Navigation Electronics Module (NEM) to give it a separate identity. In addition there were two more serial links connected to each NGCP. One of them was connected to the check out (C/O) computer on ground and meant to support all pre launch operations like automatic check out, flight parameters initializations etc. The other serial link was for tele-metering flight data. Thus evolved the architecture of OBP MKII. It consisted of two identical computing chains in which each computing chain consisted of an NEM, an NGCP and an SPM. A hardcore circuit variously known as a watchdog timer in the NGCP of the primary chain in conjunction with the self check software monitored the health of the entire chain including the health of the serial links, the NEM and the SPM of that chain. In the event of a detectable malfunction anywhere in the chain, the identically designed hot standby chain was to be switched in, without causing any disruption to the flight.

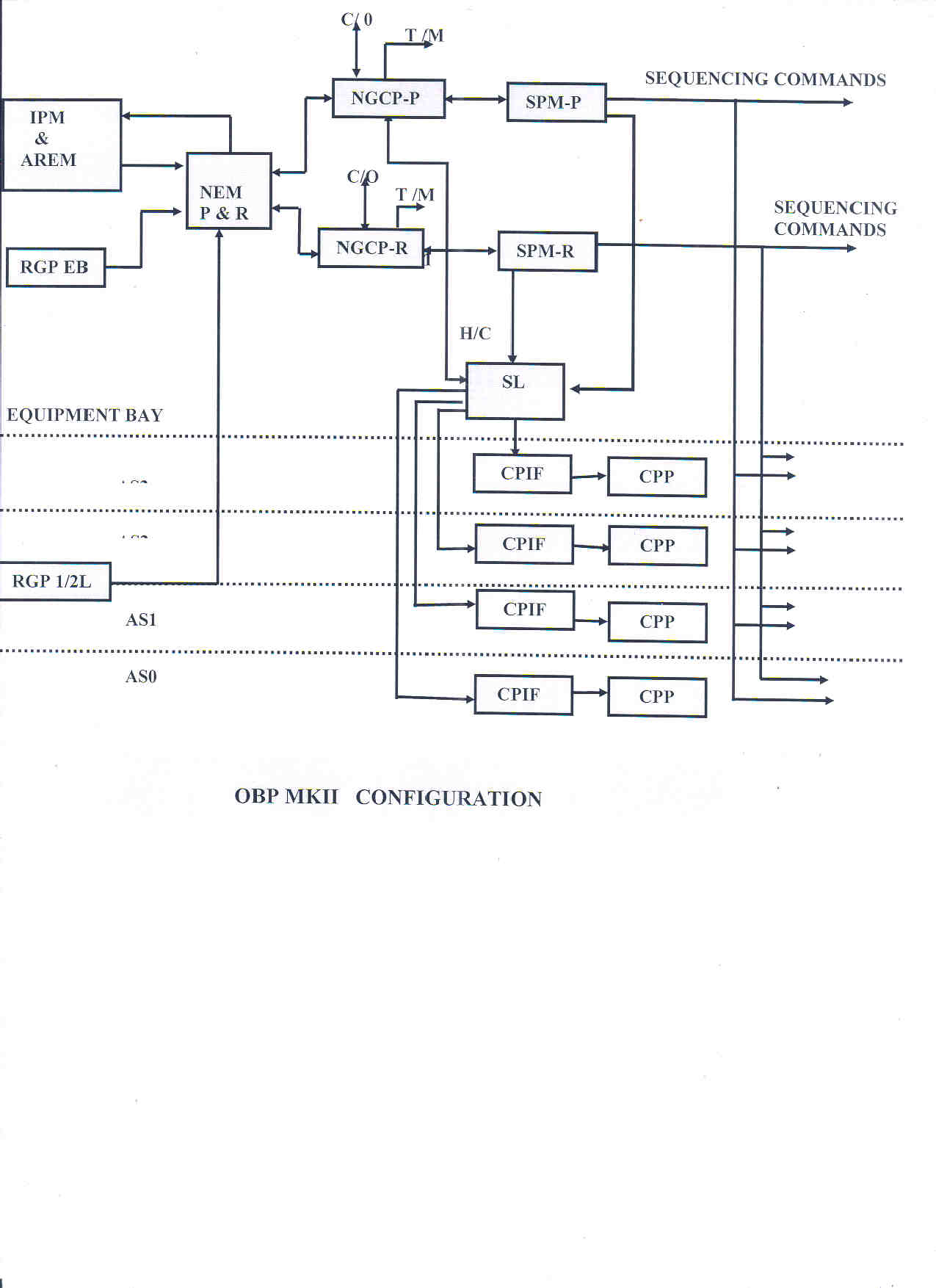
3 .The System Software.

The description of the OBP MKII system would remain incomplete without a brief mention of its system software. Since the primary aim of the system software was to manage and coordinate the hardware resources in real time, a Real Time Executive (REX) was designed to incorporate the following features.

* + Schedule execution of different tasks in real time.
  + Maintain a real time clock for the above.
  + Handle all I/O operations.
  + Keep a watch on the system health by means of a self check routine.
  + Receive and execute commands from the ground check out computer during pre launch operations.

It had three modes of operation viz. monitor mode, preflight mode and flight mode. The monitor mode is a non- real- time mode and is used for loading data from ground and also for testing different hardware modules under command from ground computer. The preflight mode and flight mode denote that the operating environment of the OBP is real time and it is executing tasks in the preflight and flight phases of the mission respectively.

The deployment of OBP MKII took place in the first two unsuccessful missions of ASLV in 1987 and 1988. Massive corrections were introduced on various aspects of the launch vehicle control system design. One of the major changes introduced was in the introduction of real time decision (RTD) making on board. This called for the design of RTD software as a part of REX support to other various application software tasks. There has been no looking back since. The first successful flight of ASLV D3 in 1993 was a day which all those associated with the development of OBP in VSSC would always look back upon as one of the most joyful moments in their lives. The last deployment of OBP MKII was in 1994 in the ASLV D4 mission. By this time the overwhelming computational requirements of the more advanced Polar Satellite Launch Vehicle (PSLV) had emerged and it was time to move on from OBP MKII to OBP MKIII.



OBP MKIII

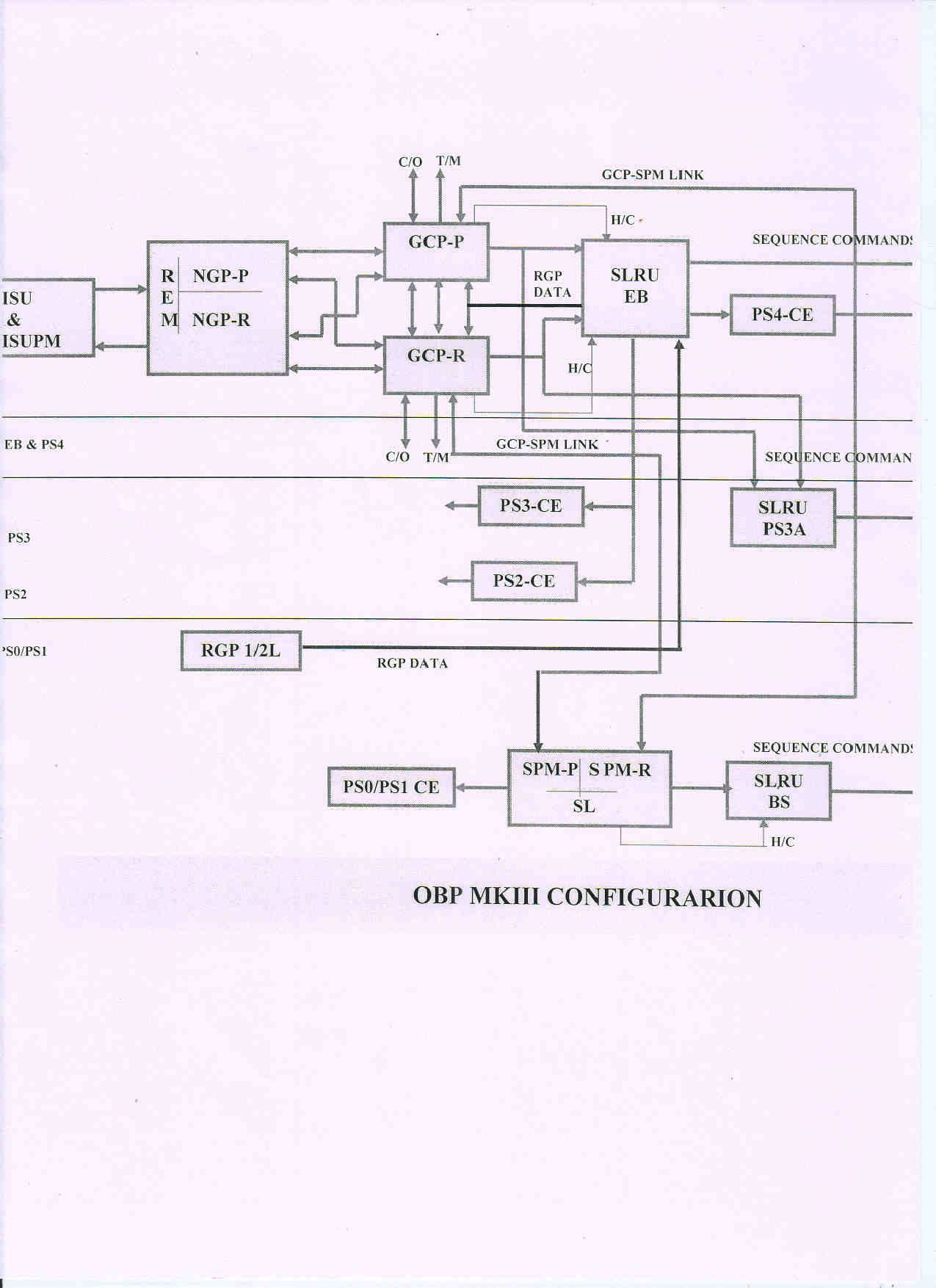
Towards the end of the 1980s, it was clear that to support the more ambitious PSLV which was to have a strapped down inertial navigation system as compared to a stabilized platform based inertial navigation system in the ASLV, a more powerful OBP had to be developed. By that time the more powerful 16 bit microprocessor M68000 from Motorola had been introduced in the market. The RAM chips also had to be upgraded to the higher capacity 2K\*8, 6516. In fact some preliminary hardware design had already been done as a part of the Automatic Payload Control Rocket Experiment (APCREX) project. A point debated over some period of time was whether the OBP MKIII like its predecessor would have a single NGCP to cater to all the major computational needs of the program or not. A school of thought, advocating a separate processor for the navigation functions alone had emerged. This was mostly to have an autonomous inertial navigation system complete with its own computer. This would enable the navigation system to be tested on its own without being coupled with the guidance and control system of the PSLV. The OBP MKIII adopted this approach and in hindsight it seems to have been a very wise decision because over the years the computational requirements exploded and a single CPU would not have been able to do the jobs, which are currently shared between the two processors, the Navigation Processor (NGP) and the Guidance and Control Processor (GCP)

1. The Architecture and Software.

The basic attributes of the architecture such as

* + use of optically isolated serial links to carry out inter processor communication.
  + use of an SPM for data distribution to stages
  + two identical computing chains, one primary and the other redundant acting as a hot standby
  + two periodicities of computation, viz. a major cycle every 500 miliseconds and a minor cycle every 20 miliseconds
  + C/O and T/M links from the main computers
  + REX which schedules the execution of real time tasks among other things were all derived from the experiences of OBP MKII.

Thus the OBP MKIII in each chain consists of an NGP, which is interfaced with the inertial sensors at its input and connected by a serial link to a GCP at its output. These are located in the equipment bay (EB) of the PSLV. The SPM which distributes output data to the lower stage actuators is located in the base shroud and receives its inputs from the GCP via an optically isolated serial link. The per chain configuration of OBP MKIII is therefore an NGP, a GCP and an SPM. A hardcore circuit in the GCP along with REX self check software determine which unit in the primary chain is faulty. However a significant difference between OBP MKII and OBP III is with respect to fault tolerance. It can be explained as follows.



In OBP MKII a fault in any unit in the primary chain caused the entire chain to be discarded and replaced automatically by the redundant chain. In OBP MKIII this replacement is limited to the individual unit which has become faulty. Thus if for example the SPM (P) i.e. the SPM in the primary chain develops a fault then SPM (P) would be replaced by SPM (R) but the other elements of the primary chain namely the NGP (P) and GCP (P) would be still functional. In other words SPM (R) would receive its inputs from GCP (P) rather than GCP (R). This type of a system is known as dual redundant scheme with cross strapped elements between the primary and the redundant chains. This increases the hardware utilization manifold in the sense that in the event of a failure of one of the elements in the primary chain only the corresponding element in the redundant chain is brought into the computational loop without losing the other elements in the primary chain. This is as if the two chains are cross connected or cross strapped. It is to be appreciated that this concept of cross strapped dual redundant scheme brought along with it an order of magnitude increase in the complexity of software and test systems. But then these challenges were met and till my superannuation in 2002 barring the first unsuccessful flight of PSLVD1 in 1991, the OBP MKIII continued to serve ISRO’s launch vehicle programs of PSLV and GSLV.

1. **Epilogue**

I have tried to describe the work carried out at VSSC in the area of avionics computer systems during a period when the technogical advances of today were unheard of .But we knew that the USA had in1969 used the Saturn V rocket to put astronauts on the moon. They had done so using computer technology which must have been yet more primitive. What we possessed then was the basic will to succeed. We had neither any formal training in Computer Science and more profoundly we were all products of an education system that was fully indigenous, a system that had taught us to learn on our own rather than committing to heart a few basic theories. We were not afraid to question our own beliefs if we were not convinced. In all this we had a set of brilliant men who did not impose their leadership on us but showed us the way by practicing what they preached. I have no hesitation in admitting that had it not been for these superb gentlemen we would not have succeeded in our mission objectives. It is the quality ambiance created by them that has made the ISRO what it is today.

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